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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,649	04/14/2004	Takashi Kurihara	1076.1094	4917

21171 7590 07/28/2006

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,649	KURIHARA ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *16-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,11-13 and 20-25* is/are rejected.

7)☒ Claim(s) *8-10, 14, and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application 10/823,649 filed on 04/14/2004 and Response to Election/Restriction filed on 05/26/2006, claims 1-25 are spending.

Claims 1-15 and 20-25 have been selected without traverse.

Claims 16-19 have been withdraw from consideration. However, Applicant is advised to cancel these claims (non-elected) in the next communication.

Claim Objections

2. Claims 12, 20, and 25 are objected to because of the following informalities: after "A method for estimating" changes "the size" to "sizing". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7, 11-13, and 20-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujine et al. (hereinafter as "Fujine") (US Patent 6,247,162).

6. With respect to claims 1, 21, and 24, Fujine discloses a method, an apparatus, and a recording medium *(The Abstract)* comprising computer instructions stored thereon for determining quantity and positions of a plurality of power supply pads *(power supply terminal)* in a semiconductor integrated circuit including a core section *(functional block or block) (figures 8, 11, and 12, element [21])* provided with a plurality of nodes *(figures 11 and 12, elements [N1-N9])*, each power supply pad *(power supply terminal) (figures 9-11, elements [T1, T2, T3, and T4])* being connected to the core section via an IO buffer *(resistors) (figure 11, elements [R3, R7, R10, R13, and R16])*, wherein each IO buffer has a predetermined current capacity *(predetermined current consumption) (col. 1, ll. 17-22)*, the method, the apparatus, and the computer instructions when executed by a computer performing steps *(figure 1)* including:

(Claim 21) storage device which stores power consumption information of the core section and power supply wire resistance information, including resistances between the nodes *(first and second files) (figures 1-4 and col. 4, ll. 28-52)*; and

(Claim 21) a data processor in communication with the storage device, in which the data processor *(figure 1, col. 4, ll. 10-27)*;

(Claims 1, 21, and 24) performing a power supply network analysis *(figure 2, step [S3] as figure 5)* of the core section *(functional block or block)* based on power consumption information the core section and power supply wire resistance information *(input design information) (figure 2, step [S1] as figure 3 and col. 5, ll. 20-35)*, which includes resistances between the nodes *(figure 11, resistors R1-R17 between the*

nodes N1-N9), to calculate voltage values of the nodes *(figure 2, step [S3] as figure 5 and col. 6, ll. 2-17)*;

(Claims 1, 21, and 24) calculating current values between the nodes from the voltage values of the nodes and the resistances between the nodes *(figure 2, step [S3] as figure 5, step [S3a] and col. 6, ll. 2-8; and col. 8, ll. 3-6)*;

(Claims 1, 21, and 24) calculating current values of the power supply pads from the current values between the nodes *(calculating the current consumption in each power supply terminal) (figure 2, step [S3] as figure 5, step [S3b] and col. 6, ll. 9-17 and col. 7, ll. 35-56)*;

(Claims 1, 21, and 24) determining whether the current value of each of the power supply pads exceeds the current capacity the associated IO buffer *(figure 2, step [S4] as figure 6, step [S4a] and col. 6, ll. 18-27, and col. 8, ll. 20-22 and ll. 26-31)*; and

(Claims 1, 21, and 24) eliminating or adding at least one power supply pad *(change/modify the structure)* in accordance with the result of the determination *(figure 2, step [S4] as figure 6, step [S4b] and col. 6, ll. 28-52, and col. 8, ll. 22-26 and ll. 31-32)*.

7. With respect to claim 2, Fujine discloses the method according to claim 1, wherein said calculating voltage values of the nodes includes calculating IR drop values between the nodes based on the voltage value each node and suspending subsequent processing when any one of the calculated IR drop values exceeds a predetermined maximum IR drop value *(col. 5, ll. 6-20, col. 6, ll. 9-17, and col. 8, ll. 3-33)*.

8. With respect to claim 3, Fujine discloses the method according to claim wherein said performing a power supply network analysis includes modeling the core section as a plurality of equivalent circuits electrically equivalent to one another, each equivalent circuit including a resistor and a current source, and performing the power supply network analysis on the modeled core section *(col. 1, ll. 35-49, col. 5, ll. 44-67-col. 6, ll. 1-17, and col. 7, ll. 59-67-col. 8, ll. 1-14)*.

9. With respect to claim 4, Fujine discloses the method according to claim 1, wherein said performing a power supply network analysis includes taking into consideration bias of power supply wire density the core section *(col. 6, ll. 44-52 and col. 8, ll. 15-33)*.

10. With respect to claim 5, Fujine discloses the method according to claim 1, wherein said performing a power supply network analysis includes taking into consideration bias of power consumption of the core section *(power consumption ratio in each power terminal of each block and the total current consumption of the entire block)(col. 8, ll. 34-40)*.

11. With respect to claim 6, Fujine discloses the method according to claim 1, wherein said performing a power supply network analysis includes taking into consideration bias of the current values of the power supply pads *(the current consumption in each power supply terminal is considered)(col. 8, ll.41-47)*.

12. With respect to claim 7, Fujine discloses the method according to claim 1, wherein the designed semiconductor integrated circuit is provided with a plurality of pads including the power supply pads, the method further comprising: pads as power

supply pads at which the potential is the same *(col. 1, ll. 50-54; and figure 5, and col. 6, ll. 1-17)*, wherein said eliminating or adding at least one power supply pad includes eliminating a power supply pad of which current value is less than the current capacity *(figure 2, step [S4] as figure 6, step [S4b] and col. 6, ll. 28-52, and col. 8, ll. 22-26 and ll. 31-32)*.

13. With respect to claim 11, Fujine discloses a method provisionally determining quantity and positions of a plurality of power supply pads before detailed design of a semiconductor integrated circuit *(the power wiring structure decision)*, wherein the semiconductor integrated circuit includes a core section *(functional block or block) (figures 8, 11, and 12, element [21])* provided with a plurality of nodes *(figures 11 and 12, elements [N1-N9])* and a plurality of power supply pads *(power supply terminals) (figures 9-11, elements [T1, T2, T3, and T4])*, the method comprising:

initially defining all of the pads as power supply pads at which the potential is the same *(col. 1, ll. 50-54; and figure 5, and col. 6, ll. 1-17)*;

performing a power supply network analysis *(figure 2, step [S3] as figure 5)* of the core section based on power consumption information the core section and power supply wire resistance information *(input design information including external power wiring layout information, block layout information, and block current consumption value) (col. 2, ll. 27-45; figure 2, step [S1] as figure 3 and col. 5, ll. 20-35)*, which includes resistances between the nodes *(figure 11, resistors R1-R17 between the nodes N1-N9)*, to calculate voltage values of the nodes *(figure 2, step [S3] as figure 5 and col. 6, ll. 2-17)*;

calculating current values between the nodes from the voltage values of the nodes and the resistances between the nodes *(figure 2, step [S3] as figure 5, step [S3a] and col. 6, ll. 2-8, and col. 8, ll. 3-6)*;

calculating current values of the power supply pads from the current values between the nodes *(calculating the current consumption in each power supply terminal) (figure 2, step [S3] as figure 5, step [S3b] and col. 6, ll. 9-17 and col. 7, ll. 35-56)*;

determining whether there is a power supply pad for which current value is less than or equal to a predetermined current capacity *(figure 2, step [S4] as figure 6, step [S4a] and col. 6, ll. 18-27, and col. 8, ll. 20-22 and ll. 26-31)*; and

adding a new power supply pad near a power supply pad for which current value exceeds the predetermined current capacity *(figure 2, step [S4] as figure 6, step [S4b] and col. 6, ll. 28-36, and col. 8, ll. 20-22 and ll. 26-31)*, and assigning a power supply pad as another type pad when the current value of that power supply pad is less than or equal to the predetermined current capacity *(figure 2, step [S4] as figure 6, step [S4b] and col. 6, ll. 37-52, and col. 8, ll. 22-26 and ll. 31-52)*.

14. With respect to claims 12, 22, and 25, Fujine discloses a method, an apparatus, and a recording medium *(the Abstract)* comprising computer instructions stored thereon estimating the size of a core section semiconductor integrated circuit, wherein the core section includes a plurality of nets, each including a plurality of wires *(the layout data includes the layout data of plurality function blocks and layout of external power wiring for supplying power to each function block) (col. 4, ll. 31-34 and figure 8, 11, and 12 see*

the descriptions), the computer instructions when executed by a computer performing steps including:

(Claim 22) a storage device which stores circuit information and a layout parameter that are used to design the semiconductor integrated circuit *(first and second files) (figures 1-4 and col. 4, ll. 28-52)*;

(Claim 22) a data processor in communication with the storage device, in which the data processor *(figure 1, col. 4, ll. 10-27)*:

(Claims 12, 22, and 25) calculating the total net length of the wires of the nets and usable channel length the core section by referring to circuit information and a layout parameter that are used to design the semiconductor integrated circuit *(input design information including external power wiring layout information, block layout information, and block current consumption value) (col. 2, ll. 27-45; figure 2, step [S1] as figure 3 and col. 5, ll. 20-35)*, the total net length being the sum of the lengths of a plurality of first wires extending predetermined first direction *(figures 11-12, wire connects nodes [N7-N8] in horizontal direction)* and the lengths a plurality of second wires extending in a second direction perpendicular to the first direction *(figures 11-12, wires [A1 and A2 (vertical) connect nodes [N9-N10] and [N8-N2], respectively in vertical direction and perpendicular to wire of nodes [N7-N8])*, and the usable channel length being the sum of a channel length in the first direction and a channel length in the second direction *(figures 9-10, channel length of [T1-T4])*;

(Claim 12) calculating the total length of the first wires *(figures 11-12, wire connects nodes [N7-N8])*;

(Claim 12) calculating the total length of the second wires *(figures 11-12, wires [A1 and A2 (vertical) connect nodes [N9-N10] and [N8-N2], respectively)*; and

(Claims 12, 22, and 25) determining the size of the core section that satisfies conditions the total net length being less than or equal to the usable channel length, the total length of the first wires being less than or equal to the channel length in the first direction, and the total length of the second wires being less than or equal to the channel length in the second direction *(col. 4, ll. 30-41, col. 6, ll. 44-52, and col. 8, ll. 20-60)*.

15. With respect to claim 13, Fujine discloses the method according to claim further comprising: determining whether the conditions are satisfied *(figure 6, step [S4a])*; and changing the layout parameter and repeating said calculating the total net length of the wires of the nets and usable channel lengths, the total length of the first wires, and the total length of the second wires, and said determining until the conditions are satisfied *(figure 2, step [S4] as figure 6, step [S4b] and col. 6, ll. 28-52; and col. 8, ll. 20-52)*.

16. With respect to claims 20 and 23, Fujine discloses a method and an apparatus for designing a semiconductor integrated circuit provided with a core section *(functional block or block) (figures 8, 11, and 12, element [21])* and plurality of power supply pads, the core section including a p plurality of nodes and a plurality of nets, each net having a plurality of wirers and each of the power supply pads being connected to the core section via an IO buffer having a predetermined current capacity *(col. 1, ll. 17-22)*, the method and the apparatus comprising:

(Claim 23) storage device which stores power consumption information of the core section, power supply wire resistance information, which includes resistances between the nodes, and circuit information and a layout parameter that are used design the semiconductor integrated circuit *(first and second files) (figures 1-4 and col. 4, ll. 28-52)*; and

(Claim 23) data processor in communication with the storage device, in which the data processor *(figure 1, col. 4, ll. 10-27)*:

(Claims 20 and 23) calculates the total net length of the wires of the nets and the usable channel length of the core section by referring to the circuit information and the layout parameter, the total net length being the sum of the lengths plurality of first wires extending predetermined first direction *(input design information including external power wiring layout information, block layout information, and block current consumption value) (col. 2, ll. 27-45; figure 2, step [S1] as figure 3 and col. 5, ll. 20-35)* and the lengths of plurality of second wires extending a second direction perpendicular to the first direction *(figures 11-12, wires [A1 and A2 (vertical) connect nodes [N9-N10] and [N8-N2], respectively in vertical direction and perpendicular to wire of nodes [N7-N8])*, and the usable channel length being the sum of a channel length in the first direction and a channel length in the second direction *(figures 9-10, channel length of [T1-T4])*;

(Claims 20 and 23) determines the size of the core section that satisfies conditions of the total net length being less than or equal to the usable channel length, the total length the first wires being less than or equal to the channel length in the first

direction, and the total length of the second wires being less than or equal to the channel length in the second direction *(col. 4, ll. 30-41, col. 6, ll. 44-52, and col. 8, ll. 20-60)*;

(Claims 20 and 23) performs a power supply network analysis of the core section *(functional block or block) (figures 8, 11, and 12, element [21])* by referring the determined size of the core section, the power consumption information, and the power supply wire resistance information *(input design information including external power wiring layout information, block layout information, and block current consumption value) (col. 2, ll. 27-45; figure 2, step [S1] as figure 3 and col. 5, ll. 20-35)* to calculate voltage values of the nodes *(figure 2, step [S3] as figure 5 and col. 6, ll. 2-17)*;

(Claims 20 and 23) calculates current values between the nodes from the voltage values of the nodes and the resistances between the nodes *(figure 2, step [S3] as figure 5, step [S3a] and col. 6, ll. 2-8, and col. 8, ll. 3-6)*;

(Claims 20 and 23) calculates current values of the power supply pads from the current values between the nodes *(calculating the current consumption in each power supply terminal) (figure 2, step [S3] as figure 5, step [S3b] and col. 6, ll. 9-17 and col. 7, ll. 35-56)*;

(Claims 20 and 23) determines whether there power supply pad for which current value exceeds the current capacity of the associated IO buffer *(figure 2, step [S4] as figure 6, step [S4a] and col. 6, ll. 18-27, and col. 8, ll. 20-22 and ll. 26-31)*; and

(Claims 20 and 23) eliminates or adds a power supply pad in accordance with the result of the determination to determine the quantity and locations of the power

supply pads *(figure 2, step [S4] as figure 6, step [S4b] and col. 6, ll. 28-52; and col. 8, ll. 20-52).*

Allowable Subject Matter

17. Claims 8-10 and 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

18. The following is a statement of reasons for the indication of allowable subject matter: the prior art made of record does not teach or fairly suggest of the inventive step comprising:

(as claim 8) determining whether a completion condition is satisfied after deleting the at least one power supply pad.

(as claim 9) eliminating or adding at least one power supply pad includes checking whether deletion of every one of the power supply pads excluding the reference pad is possible.

(as claim 14) calculating an average path length of the wires in each calculating the net length of each net based on the average path length and fan-out of each net to calculate the total net length of the nets and the aspect ratio of each circuit block.

(as claim 15) calculating the usable channel length of each wire layer from the routing prohibition channel length and a maximum channel usage rate, which is in accordance with the area of the estimated area, to calculate the total usable channel length the wire layers.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Banno et al. (US Patent 6,763,511) disclose a method for optimizing layout of a semiconductor circuit design, which is including macro cells and wiring group in horizontal and vertical directional in the circuit layout.

Ditlow et al. (US Patent 6,868,374) disclose a method of testing the compliance of power distribution of I/O circuit in a semiconductor chip with voltage drop (IR) and electromirgation (EM) limits based on power distribution network analysis.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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